

Electronics developments in Orsay, France

Albrecht Karle

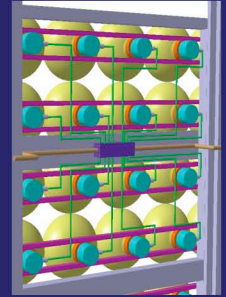
Summary from a visit in Orsay,

Thanks to

Jean-Eric Campagne, Joël Pouthas and the
Orsay team.

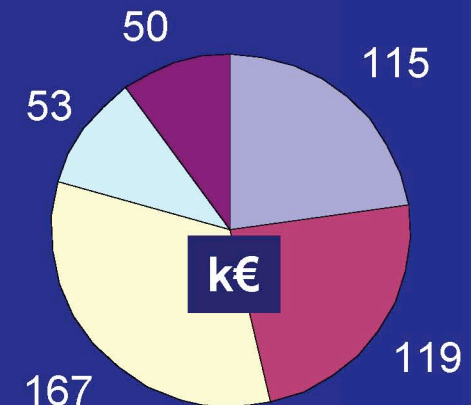
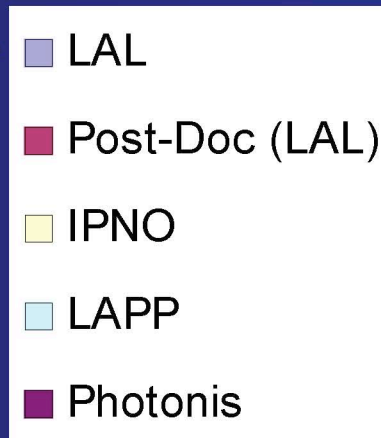
The following slides are (mostly) taken from
presentations by the Orsay team during the visit
in January.

PMm² ANR (2007-2009)



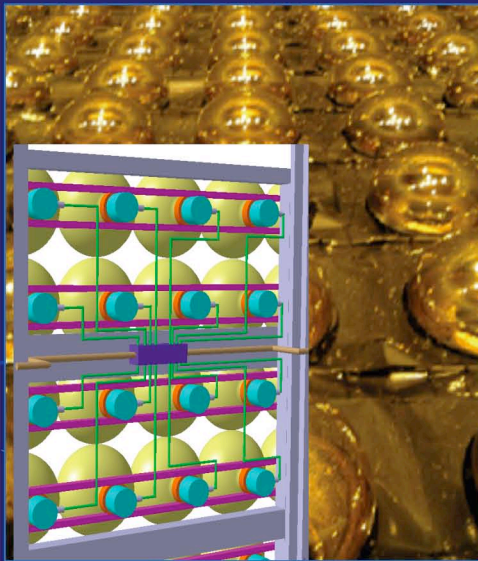
- **LAL**: front end electronics + water tight box
- **IPNO**: photodetector tests + mechanics + integrated electronic board
- **LAPP**: Data network (electronics + cables + protocol but not DAQ)
- **Photonis**: PMTs provider

Funded **500k€/3yrs** (1 post-doc included) designed to involve **5FTE Engineers**
And in fact **~20p** participate to our “monthly” meeting.



*:95% of the requested money

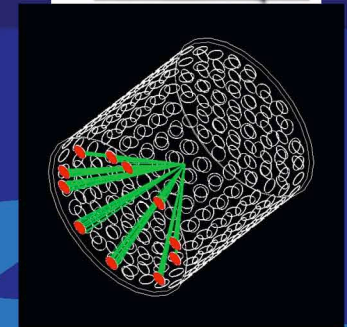
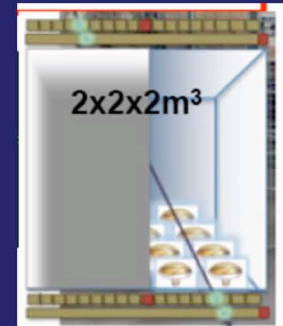
<http://pmm2.in2p3.fr>



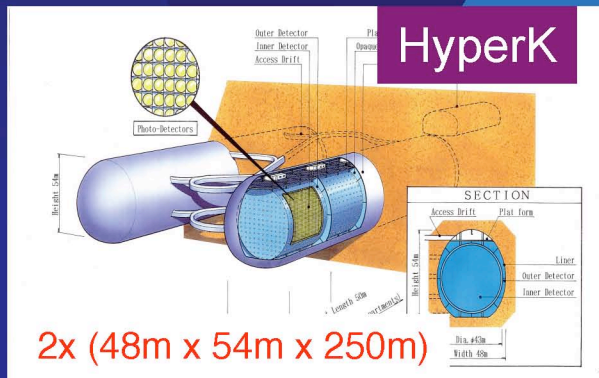
« PMm² » R&D



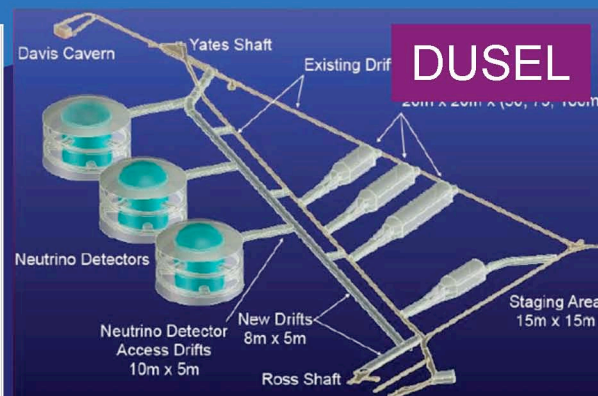
MEMPHYNO Prototype Series



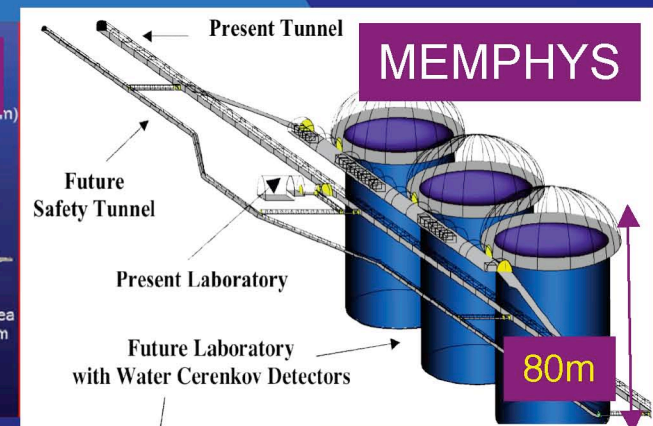
- Nucleon decay
- ν properties
- ν from supernova



Japan



USA

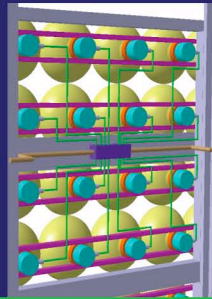


EU

J.E Campagne 19-20/01/09

PMM²

Our concept
(2007)



Realisation
(2008)

Integration
“demonstrator”
(2009)



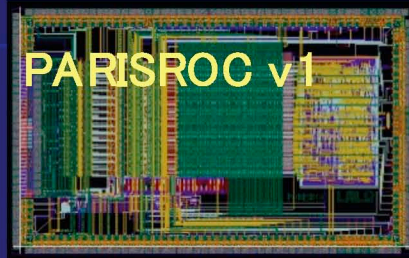
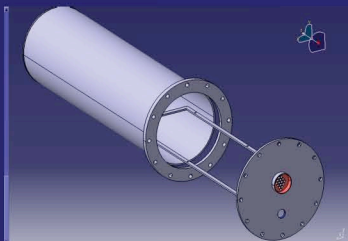
XP1812

12" 10b

IPNO CAO

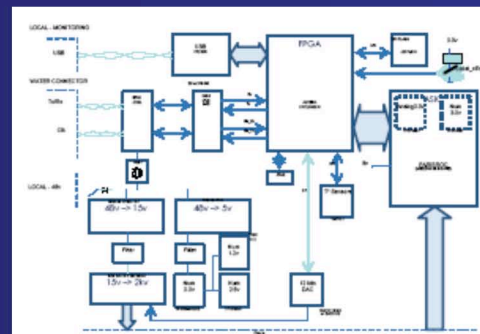
Photonis Electrostatic et
realisation (Sept. 08)
And cables, water tightness

LAL water
tight box @
10b under
design (Dec.
08)

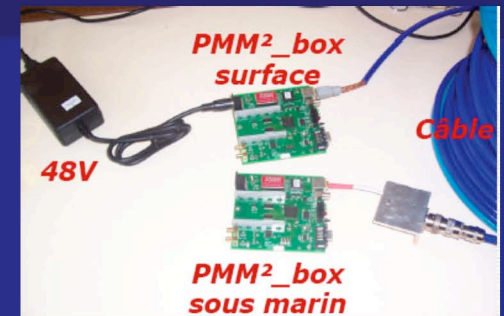


PARISROC v1

LAL ASIC SiGe 0.35 μ m
(received Oct. 08) under
test till Dec. 08



IPNO integration board
under design

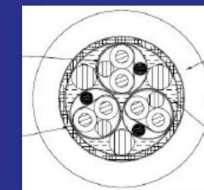


PMM²_box
surface

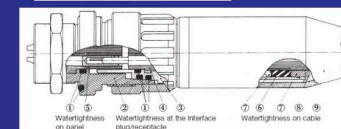
48V

Câble

PMM²_box
sous marin



Hydrocable
System



Souriau



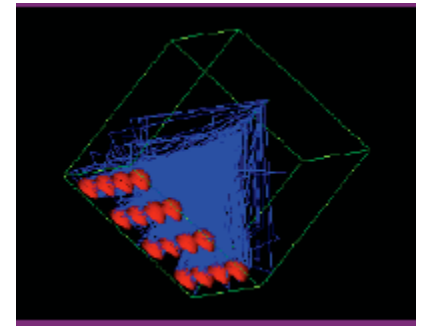
IPNO BNL vessel (Juil. 08) to test all the
components under pressure @ 10b (Early
08)

LAPP

Triggrless Data network
10Mbs to the “surface” +
synchro GPS + puissance
(Power over Ethernet)
Tests of submarine cables
(photo: Hydrocable System
Oct. 08) & connectors.

Schedule: ready Q3 09'

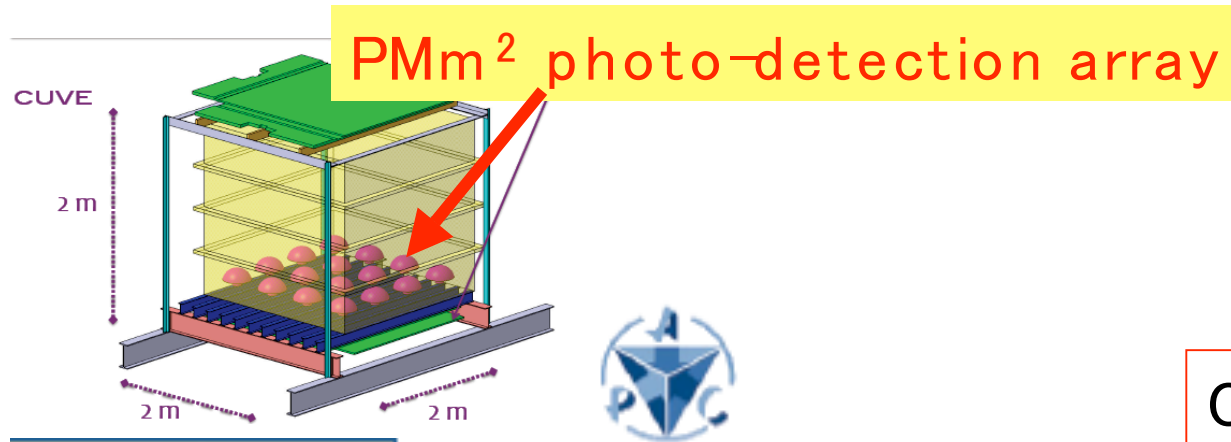
MEMPHYNO-I



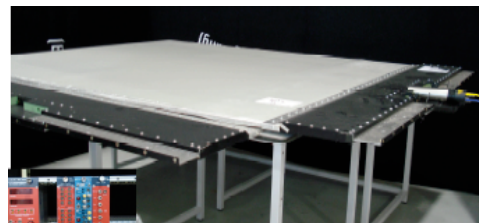
5 GeV muons

Foreseen Tests

Complet DAQ chain
Trigger threshold
Self trigger capability
Some Tracking



PEHD vessel
2 m x 2 m x 2 m
Recycling water



Hodoscope from OPERA
Using MAROC2 LAL board

Operated first at APC, then at
LSM Fréjus and may be at CERN
on a test beam.

MEMPHYNO-I

= Test system with
16 PMTs and readout

- The purpose of this device is to perform some basic tests on post-PMm2 although it will not be possible to register proper Cerenkov cone (ČČ) and only **one PMm²** device will be used limiting the read out tests that are key issue as: **synchronisation of several devices, measurement *in situ* of the triggerless data flux, online reconstruction of ČČ among PM dark current noise...**

MEMPHYNO-II

- bigger WČ to be operated in a new hall of the next extension of the LSM. Call for LoI mid-2009 workshop.
- The purpose is to register in situ all kind of events (passing muons, natural radioactivity electrons, photons and neutrons) and to reconstruct the associated ČC. From recent mails with B. Svoboda, there is interest of Gd loading.
- This imply to setup a complete acquisition chain with multi-PMm² devices all synchronised

PArISROC description (I)

- Complete front-end chip with 16 channels

Sent in fabrication in **June 2008**

Technology : **AMS SiGe 0.35 μm**

- Characteristics :

- 16 inputs preamplifier
 - Variable gain : $1 \rightarrow 8$ (4bits) (common on 16 channels)
 - PMTs gain adjustment by a factor 4 (8 bits) (channel by channel)
 - Input dynamic range : $0 \rightarrow 300$ pe ($0 \rightarrow 50\text{pC}$)
 - Good linearity (1%)
- **16 trigger outputs:**
 - Fast shaper ($\tau=15\text{ns}$)
 - Low offset discriminator
 - Threshold provided by common 10bit DAC +4bit DAC/ch. (1/3 pe)
 - "OR" of 16 triggers output
- **1 digitized and multiplexed charge output :**
 - Dynamic range : $0 \rightarrow 300$ pe
 - Slow shaper with variable shaping time ($\tau=50\text{ns}, 100\text{ns}, 200\text{ns}$)
 - SCA with depth 2



PArISROC description (II)

- Coarse time measurement (timestamp) :
 - 24-bit counter @ 10MHz
 - Step : 100ns

- 12-bit ADC for charge and fine time measurement :
 - Wilkinson type ADC
 - T&H on slow shaper for charge measurement
 - T&H on TDC ramp (100ns) for fine time measurement
 - 2 discriminators with 12 bit ramp (100 μ s) as threshold

- Serialization of digital output information :
Channel number - time stamp – charge - fine time
4bits 24bits 12bits 12bits

PMm² : large photodection area

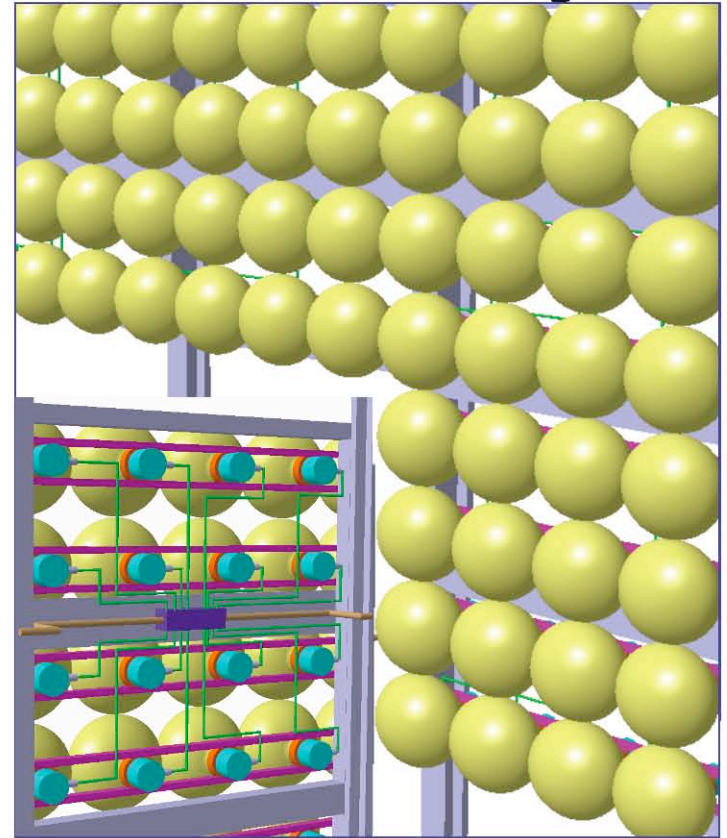


PMm2" (2006 - 2009), funded by the ANR : LAL, IPNO, LAPP and Photonis

replace large PMTs (20") by groups of smaller ones (12")

- central 16ch ASIC (PaRISROC)
- 12 bit charge + 12 bit time
- water-tight, common High Voltage
- Only one wire out (DATA + VCC)
- Target low cost
- Reuse many parts from MAROC & SPIROC

pplication : large water Cerenkov neutrino



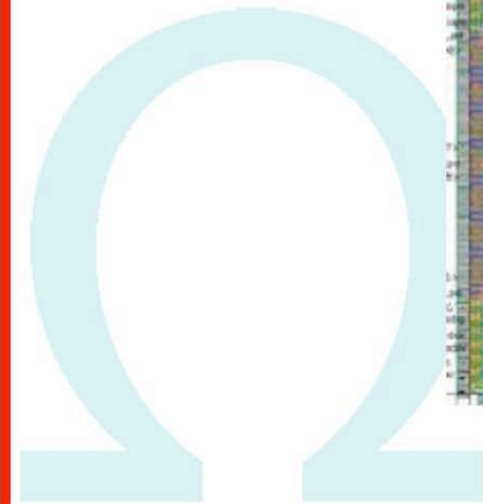
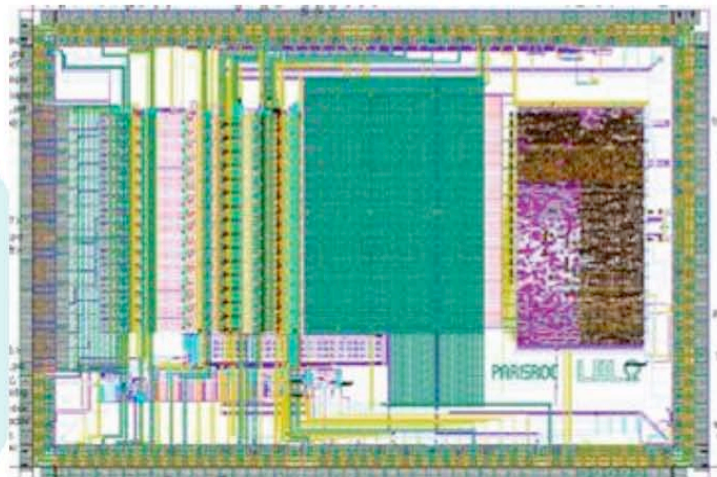
PARISROC

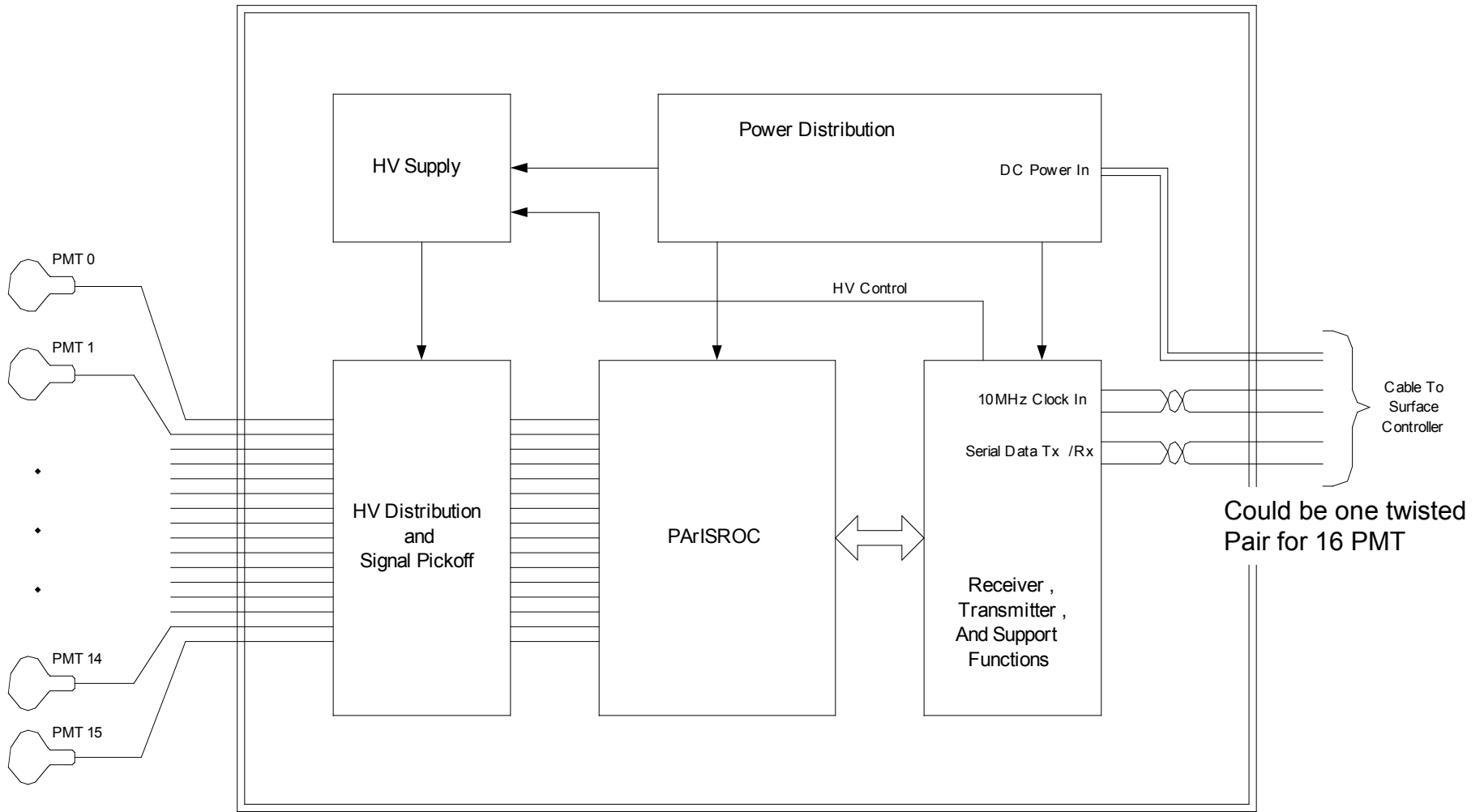
Photomultiplier Array Integrated in Sige Read Out Chip

PARISROC specifications

Omega

- Based on a complete 16 channels read out chip with dedicated for Photomultiplier array (PARISROC)
- Measurement of Charge and time

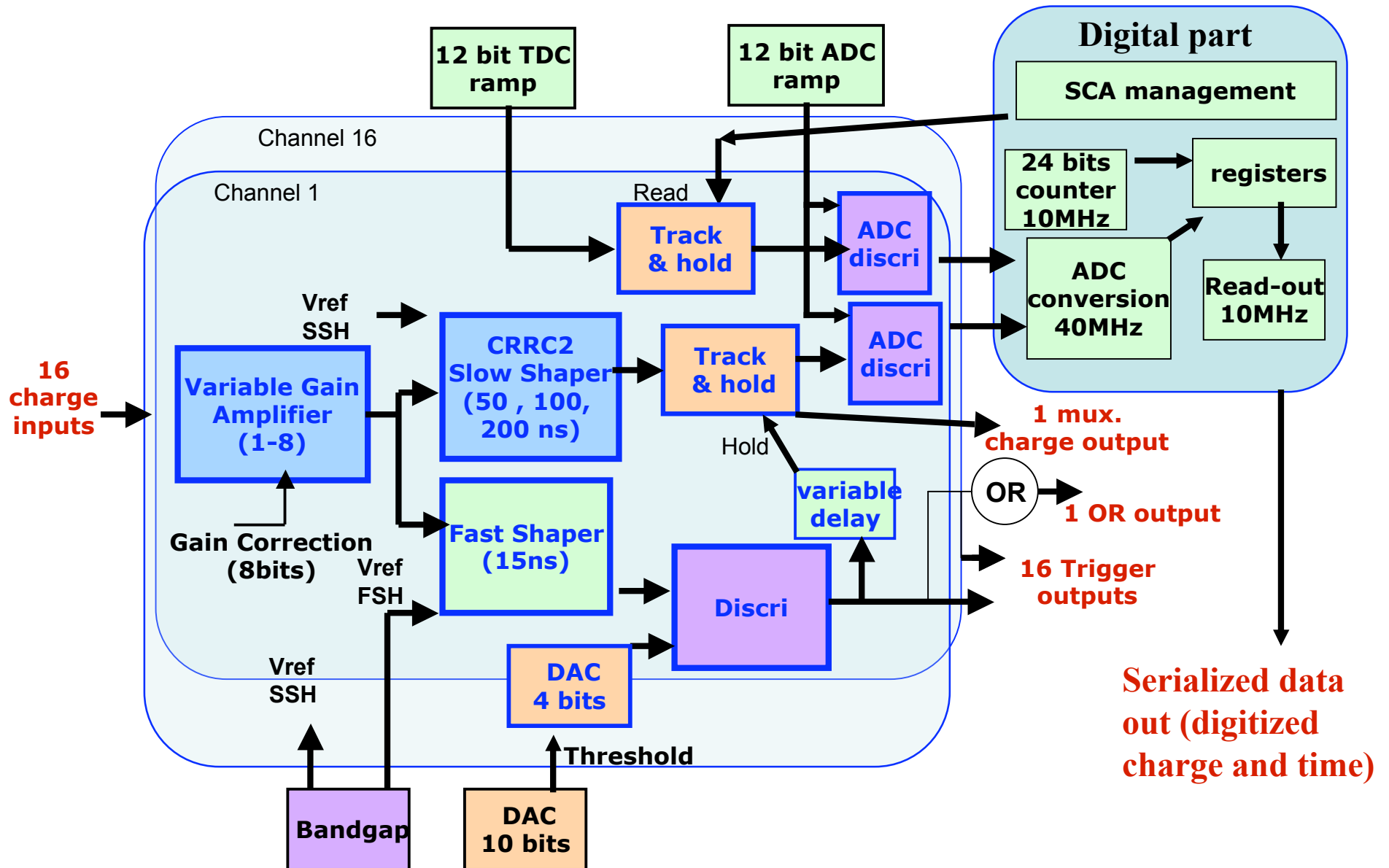




PARISROC Performs Data Acquisition on a 16-PMT Assembly For LBDUSEL



PArISROC architecture



Summary analog part

Preamplifier's Characteristics :

- 16 inputs preamplifier
- Variable gain : $1 \rightarrow 8$ (4bits) (common on 16 channels)
- PMTs gain adjustment by a factor 4 (8 bits) (channel by channel)
- Dynamic range : $0 \rightarrow 300$ pe ($0 \rightarrow 50$ pC)
- Linearity $< 1\%$ (50 pC)
- SNR = 30

Slow Shaper 's Characteristics :

- Time constant : $\tau = 50, 100, 200$ ns peaking time
- Linearity $< 0.4\%$ (55 pC)
- SNR = 5 (RC=200ns);
8 (RC=100ns);
11 (RC=50ns)

Fast Shaper 's Characteristics :

- Time constant : $\tau = 15$ ns
- SNR = 28

Discriminator 's Characteristics :

- Timewalk = 4 ns
- Threshold = 50 fC = $1/3$ pe

My summary from visit to Orsay

- ASIC chip designed at Orsay likely to meet requirements for Dusel water cherenkov PMT pulse digitization.
- Strong team at Orsay. Possibility of worldwide collaboration on water cherenkov.
- Kael Hanson at Brussels University Libre working with Orsay on DAQ software with goal of test setup.
- Possibility to set up a test system at PSL in previous IceCube temperature controlled dark test lab if collaboration considers this approach worth investigating.
- There will be a new run of the chip. Opportunity to provide feedback on requirements, eg dynamic range until April.